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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,191	11/08/2001	Daniel M. Dreps	AUS920010742US1	3560

7590 09/21/2005

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,191	DREPS ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-10* is/are allowed.

6)☒ Claim(s) *1,11, and 13* is/are rejected.

7)☒ Claim(s) *12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 07/01/2005, with respect to claim 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkar et al. (US 5,604,450).

With regard claim 1, Borkar et al. discloses a digital transmission system comprising:

first driver circuit (Fig.2 and 3, element DRVA) receiving a first data input signal (Fig.2 and 3, element COA) and generating a first driver output signal (Fig.2 and 3, element N1) in response to a clock signal (Fig.5 element EN0 – EN3, and EN0_bar – EN3_bar, where Fig.5 can be used as DRVA as shown in Fig.2 and 3 and these Enx and Enx_bar binary signals will turn DRVA on/ off so that DRVA become a driver or termination circuit and column 6 lines 46 – column 7 line 28), said first driver output coupled to a first input of a first transmission line (Fig.2 and 3, element Z_O);

a receiver circuit (Fig.2 and 3, element DIFFB) having a first receiver input coupled to a first output of said first transmission line (Fig.2 and 3, element

DIFFB "+" input terminal) and a second receiver input coupled to a reference voltage (Fig.2 and 3, element REFB); and

a first terminating network (Fig.2 and 3, element DRVB and Fig.5, and column 6 lines 46 – column 7 line 28) receiving programming signals (Fig.5 element EN0 – EN3, and EN0_bar – EN3_bar, where Fig.5 can be used as DRVB as shown in Fig.2 and 3 and these Enx and Enx_bar binary signals can be external controlled or programmed by a state machine for compensating the voltage and temperature variation) and generating a first terminating voltage with a first source impedance at a first node (Fig.1 element 24A up connection), wherein said first terminating voltage is modified in response to said programming signals while maintaining a pre-determined magnitude of said first source impedance (Fig.2 and 3 and column 3 line 3 – column 6 line 21).

- With regard claim 11, Borkar et al. further discloses a processor central processing unit (CPU) integrated circuit (IC) chip (Fig.7 element 76) operable to transmit off-chip signals (Fig.7 element 76), having circuitry (Fig.7 element 71, column 54-63) for transmitting a digital signal on a first transmission line corresponding to edges of a clock signal (Fig.7 element 81, Fig.2 and 3 element DRVA), circuitry for terminating said first transmission line in a programmable terminating voltage having a source impedance (Fig.5 element EN0 – EN3, and EN0_bar – EN3_bar, where Fig.5 can be used as DRVB as shown in Fig.2 and 3 and these Enx and Enx_bar binary signals can be external controlled or programmed by a state machine for compensating the voltage and temperature

variation), said programmable terminal voltage modified in response to first program signals (Fig.2 and 3, element DRVB and Fig.5, and column 6 lines 46 – column 7 line 28), and

circuitry for receiving said digital signal at a first receiver input coupled to said programmable terminal voltage and an output of said first transmission line (Fig.2 and 3, element DIFFB "+" input terminal), receiving a reference voltage at a second receiver input coupled (Fig.2 and 3 element REFB and "-" terminal of the DIFFB), and generating a receiver output (Fig.2 and 3, element CIB);

a random access memory (RAM) (Fig.7 element 75); and

a bus system coupling said CPU to said RAM (Fig.7 element 81), wherein said terminal voltage is modified while controlling the magnitude of said source impedance to optimize said received digital signal (Fig.2 and 3 and column 3 line 3 – column 6 line 21).

- With regard claim 13, which is a system claim related to claim 11, all limitation is contained in claim 11. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

3. Claims 2-10 and 15-17 are allowed.

4. The following is an examiner's statement of reasons for allowance.

   - The prior art fails to teach a digital transmission system/ method of Claims 2, 7, 8, and 15 that specifically comprises the following:

-- The instant application is deemed to be directed to a non-obvious improvement over the admitted prior art of the instant application and the invention patented in Pat. No. US 3,993,867, US 5,761,246, US 6,105,157, and US 6,442,644.

Claim 2, the improvement comprises that - a second driver circuit receiving said clock signal and generating a first clock output signal coupled to a second input of a second transmission line; a second terminating network generating a second terminating voltage with said first source impedance at a second node, said second node coupled to a second output of said second transmission line; a third driver circuit receiving said clock signal and ((aj) generating a second clock output signal coupled to a third input of a third transmission line, said second clock output signal a complement of said first clock output signal; a third terminating network generating a third terminating voltage with said first source impedance at a third node, said third node coupled to a third output of said third transmission line; and a filter network receiving said second and third outputs and generating said reference voltage..

Claim 7, the improvement comprises that a reference network receiving a first clock transmitted from said first IC with a second transmission line, a second clock transmitted from said first IC with a third transmission line, and said programming signals and, generating said reference voltage in response to the first and second clock, wherein said

terminating voltage is varied in response to said programming signals while maintaining a pre-determined magnitude of said first source impedance.

Claim 8, the improvement comprises that monitoring an output of said differential receiver for a quality of a received data signal; and setting said first terminating voltage at an optimized level corresponding to said quality of said received data signal.

Claim 15, the improvement comprises that said programming signals, wherein each of said first electronic switches couples said first voltage to one of said positive voltage nodes in response to a first state of said one of said programming signals and each of said second electronic switches couples said second voltage to one of said negative voltage nodes in response to a second state of said corresponding one of said programming signals.

Conclusion

5. Reference(s) US 5,872,471 and US 6,424,175 are cited because they are put pertinent to the bi-directional transmission system with programmable termination network. However, none of references teach detailed connection as recited in claim.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600